What is claimed is:

1. An automatic circuit generation system comprising:

a processing unit which is configured to receive circuit generation information required for generating a circuit, and analyzing the circuit generation information as received to generate circuit connection data and leakage current data;

an analyzing unit which is configured to receive test vectors which are used as input signals for operating the circuit, operating a circuit with the test vectors, obtaining the state(s) of each node and the probability of each state of each node as occurs in the circuit;

a leakage current estimating and input signal exchanging unit which is configured to receive said circuit generation information and the state(s) of each node and the probability of each state of each node as obtained by said analyzing unit, calculating the leakage currents of the circuit, calculating the leakage currents of the circuit in the cases where input signals to exchangable pins of the circuit are exchanged, and determining an assignment of the input signals to the exchangable pins corresponding to minimum values of the leakage currents; and

an output unit which is configured to output the netlist of the circuit in which the exchangable pins of the circuit are assigned to the input signals as generated the assignment as determined by said leakage current estimating and input signal exchanging unit.

2. An automatic circuit generation method comprising:

receiving circuit generation information required for generating a circuit, and analyzing the circuit generation information as received to generate circuit connection data and leakage current data;

receiving test vectors which are used as input signals for operating the circuit, operating a circuit with the test vectors, obtaining the state(s) of each node and the probability of each state of each node as occurs in the circuit;

receiving said circuit generation information and the state(s) of each node and the probability of each state of each node as obtained, calculating the leakage currents of the circuit, calculating the leakage currents of the circuit in the cases where input signals to

exchangable pins of the circuit are exchanged, and determining an assignment of the input signals to the exchangable pins corresponding to minimum values of the leakage currents; and

outputting the netlist of the circuit in which the exchangable pins of the circuit are assigned to the input signals as generated the assignment as determined.

3. An automatic circuit generation program embodied on a computer-readable medium for generating circuits, said program comprising:

receiving circuit generation information required for generating a circuit, and analyzing the circuit generation information as received to generate circuit connection data and leakage current data;

receiving test vectors which are used as input signals for operating the circuit, operating a circuit with the test vectors, obtaining the state(s) of each node and the probability of each state of each node as occurs in the circuit;

receiving said circuit generation information and the state(s) of each node and the probability of each state of each node as obtained, calculating the leakage currents of the circuit, calculating the leakage currents of the circuit in the cases where input signals to exchangable pins of the circuit are exchanged, and determining an assignment of the input signals to the exchangable pins corresponding to minimum values of the leakage currents; and

outputting the netlist of the circuit in which the exchangable pins of the circuit are assigned to the input signals as generated the assignment as determined.

4. An automatic circuit generation system for generating an object circuit by the use of a cell library including logic cells, said system comprising:

a node state analyzing unit which is configured to obtain combinations of input signals to exchangable input pins of a logic cell of said cell library included in said object circuit and the probabilities of the respective combinations of the input signals;

a leakage current estimating unit which is configured to determine a combination of the input signals, with which the leakage current passing through said logic cell of said cell library included in said object circuit is minimized, with reference to information about leakage

currents passing through the exchangable input pins of said logic cell of said cell library included in said object circuit; and

an output unit which is configured to output circuit information in accordance with the combination of the input signals as obtained by said leakage current estimating unit.

5. The automatic circuit generation system for generating an object circuit as claimed in claim 4 wherein the combination of the input signals is obtained by said leakage current estimating in order that the leakage current passing through said object circuit is minimized when said object circuit is inactivated in a standby state.

6. The automatic circuit generation system for generating an object circuit as claimed in claim 4 wherein the combination of the input signals is obtained by said leakage current estimating in order that the leakage current passing through said object circuit is minimized when said object circuit is operating in a normal state.

7. The automatic circuit generation system for generating an object circuit as claimed in claim 4 wherein said information of leakage currents passing through the exchangable input pins of said logic cell is obtained with reference to the circuit designs and patterns of said object circuit.

8. The automatic circuit generation system for generating an object circuit as claimed in claim 4 wherein said information of leakage currents passing through the exchangable input pins of said logic cell is obtained by measuring the actual currents passing through said object circuit.

9. An automatic circuit generation program embodied on a computer-readable medium for generating an object circuit by the use of a cell library including logic cells, said program comprising:

obtaining combinations of input signals to exchangable input pins of a logic cell of said cell library included in said object circuit and the probabilities of the respective combinations of the input signals;

determining an optimum combination of the input signals, with which the leakage current passing through said logic cell of said cell library included in said object circuit is minimized, with reference to information about leakage currents passing through the exchangable input pins of said logic cell of said cell library included in said object circuit; and

outputting circuit information in accordance with the optimum combination of the input signals as obtained with which the leakage current passing through said logic cell of said cell library included in said object circuit is minimized.

10. The automatic circuit generation program embodied on a computer-readable medium for generating an object circuit as claimed in claim 9 wherein the optimum combination of the input signals is obtained in order that the leakage current passing through said object circuit is minimized when said object circuit is inactivated in a standby state.

11. The automatic circuit generation program embodied on a computer-readable medium for generating an object circuit as claimed in claim 9 wherein said information of leakage currents passing through the exchangable input pins of said logic cell is obtained with reference to the circuit designs and patterns of said object circuit.

12. The automatic circuit generation program embodied on a computer-readable medium for generating an object circuit as claimed in claim 9 wherein said information of leakage currents passing through the exchangable input pins of said logic cell is obtained by measuring the actual currents passing through said object circuit.